

PHASE LOCKED LOOPS

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ABSTRACT: This is one of a series of white papers on systems modelling, analysis and control, prepared by Control Systems Principles.co.uk to give insights into important principles and processes in control. In control systems there are a number of generic systems and methods which are encountered in all areas of industry and technology. These white papers aim to explain these important systems and methods in straightforward terms. The white papers describe what makes a particular type of system/method important, how it works and then demonstrates how to control it. The control demonstrations are performed using models of real systems designed by our founder and senior partner Peter Wellstead, and have been developed for manufacture by TQ Education and Training Ltd in their CE range of equipment. In this white paper the computer based control and simulation tool CE2000 is used to explain one of the most widely used and misunderstood feedback circuits in the world – the phase locked loop.

1. What is a Phase Locked Loop and Why is it Important?

The Phase Locked Loop (PLL) is a feedback system. It is a basic building block used in communications systems such as mobile phones, which may contain up to 5 PLL's. Another important application is in motor speed control for optical disk drives (ODD's) as found in DVD's and CD players. The basic PLL can be analog or digital. A good review of PLL's from a control engineering perspective can be found in reference [1]. In this white paper we will describe the basic components of the PLL and show you how to build and analyse a simple PLL using the CE2000.

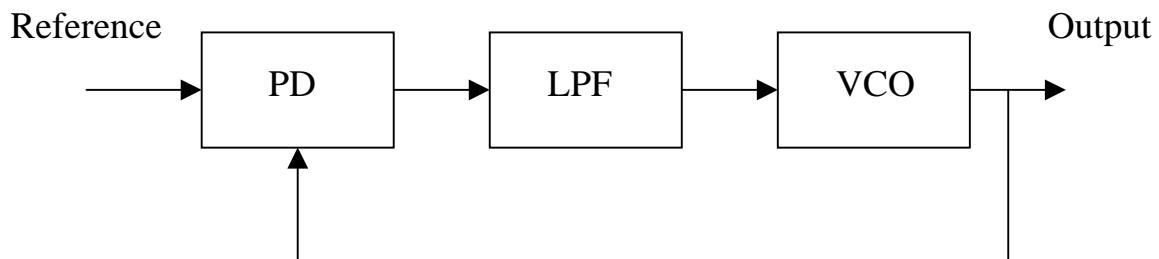


Figure 1. Basic Phase Locked Loop

The basic components of a PLL are:

- Phase detector (PD).
- Loop pass filter (LPF).
- Voltage controlled oscillator (VCO).

These three components are connected as a feedback system as shown in Figure 1. The reference signal is periodic such as sine wave (or square wave) which is compared with the output of the VCO using a phase detector. The output of the phase detector is then low pass filtered and used as a control signal to drive a voltage controlled oscillator. The idea is that the voltage-controlled oscillator will lock onto the reference signal and thus can be used to track a periodic signal as its phase and frequency varies. PLL's are inherently non-linear. The main source of non-linearity is the phase detector. However using a small signal assumption and the fact that the multiplication operator is continuous, then the basic PLL can be approximated by a linear second order system similar to a position servo.

2. Linear PLL analysis

If the input signal to the PLL is a sine wave:

$$r(t) = A \sin(\omega_r t + \theta_r)$$

and the output signal for the VCO is assumed to be

$$y(t) = \cos(\omega_y t + \theta_y).$$

The phase detector is a multiplier so the output from the phase detector is just the product of the reference and VCO signals

$$e(t) = K A \sin(\omega_r t + \theta_r) \cos(\omega_y t + \theta_y).$$

This can be expanded to give

$$e(t) = \frac{K A}{2} \left[\sin((\omega_r + \omega_y)t + \theta_r + \theta_y) + \sin((\omega_r - \omega_y)t + \theta_r - \theta_y) \right].$$

The first term on the right of the above expression is a high frequency term that is filtered out by the low pass loop filter. If we also assume that $\omega_y \approx \omega_r$, then the output from the multiplier can be approximated by:

$$e(t) = K_m \left[\theta_r - \theta_y \right].$$

The error signal is a gain multiplied by the phase difference between the reference signal and the signal from the VCO. Typically the LPF is a first order low pass filter

$$F(s) = \frac{K_f}{\tau_f s + 1}$$

and since phase is the integral of angular velocity the VCO is modelled as

$$VCO(s) = \frac{K_o}{s}.$$

Combining these transfer functions gives the loop gain

$$L(s) = \frac{K_1}{s(\tau_f s + 1)} \quad K_1 = K_m K_f K_o$$

which will be recognised as the transfer function of a position servo [2]. So the closed-loop dynamics are

$$T(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \text{where } \omega_n = \sqrt{\frac{K_1}{\tau}} \quad \text{and } \zeta = \frac{1}{2\sqrt{\tau K_1}}$$

This is a standard second order transfer function with natural frequency ω_n and damping ζ . The block diagram of the linear approximation to the PLL is shown in Figure 2. Here θ_r and θ_y are the reference signal and VCO phase shift respectively.

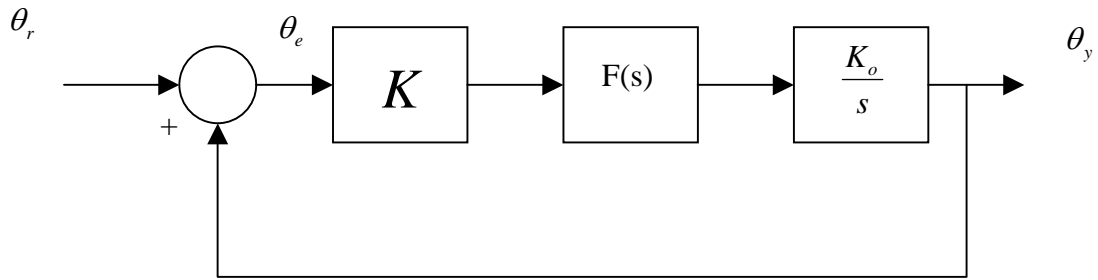


Figure 2. Linear approximation of a Phase Locked Loop

3. Implementation of a Phase Locked Loop using the CE2000 Software

A PLL can be implemented using the CE2000 software. To do this it has to be put into digital form as shown in Figure 3.0. Here each block in Figure 2.0 has been replaced by its discrete equivalent.

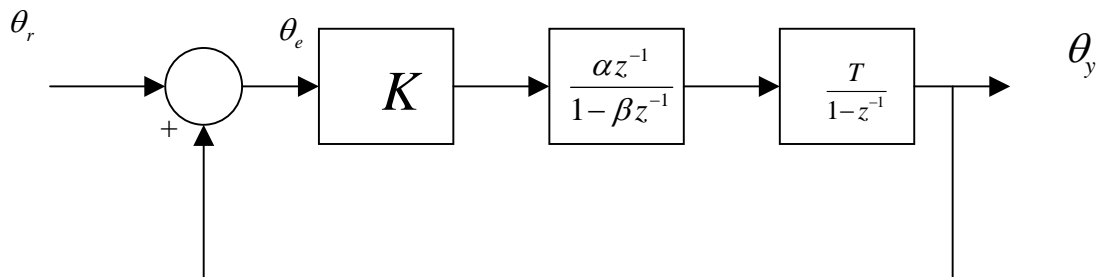


Figure 3. Digital simulation of a Phase Locked Loop

Now the loop gain is

$$L(z^{-1}) = \frac{\alpha K z^{-1}}{(1 - \beta z^{-1})(1 - z^{-1})}$$

and the closed-loop transfer function is

$$T(z^{-1}) = \frac{\alpha K z^{-1}}{\beta z^{-2} + (\alpha K - \beta - 1)z^{-1} + 1}, \quad T(z^{-1}) = 1$$

Initially we use $K = 1$, $\beta = 0.95$ and $\alpha = 1 - \beta$ when running the CE2000 program.

A CE2000 implementation of a PLL is shown in Figure 4. In Figure 4 the reference oscillator is initially set to 1.5 Hz using a constant input. The PLL then generates a feedback signal so that the VCO locks onto this reference signal by generating a signal of the same frequency phase shifted by 90 deg or pi/4 radians. A scope block is used to generate a Lissajous figure using the reference and VCO. When the VCO is locked to the reference the Lissajous figure will be a circle. The frequency of the reference signal can now be increased slightly and the PLL will relock the VCO to the reference signal. Only small increments in the frequency can be made otherwise the VCO will fail to lock to the reference. It is interesting to observe that this simple PLL will also lock to reference signals with different waveforms

for example a square wave or a triangular wave. This shows how a PLL can be used as a filter by locking onto harmonics of a complex periodic signal.

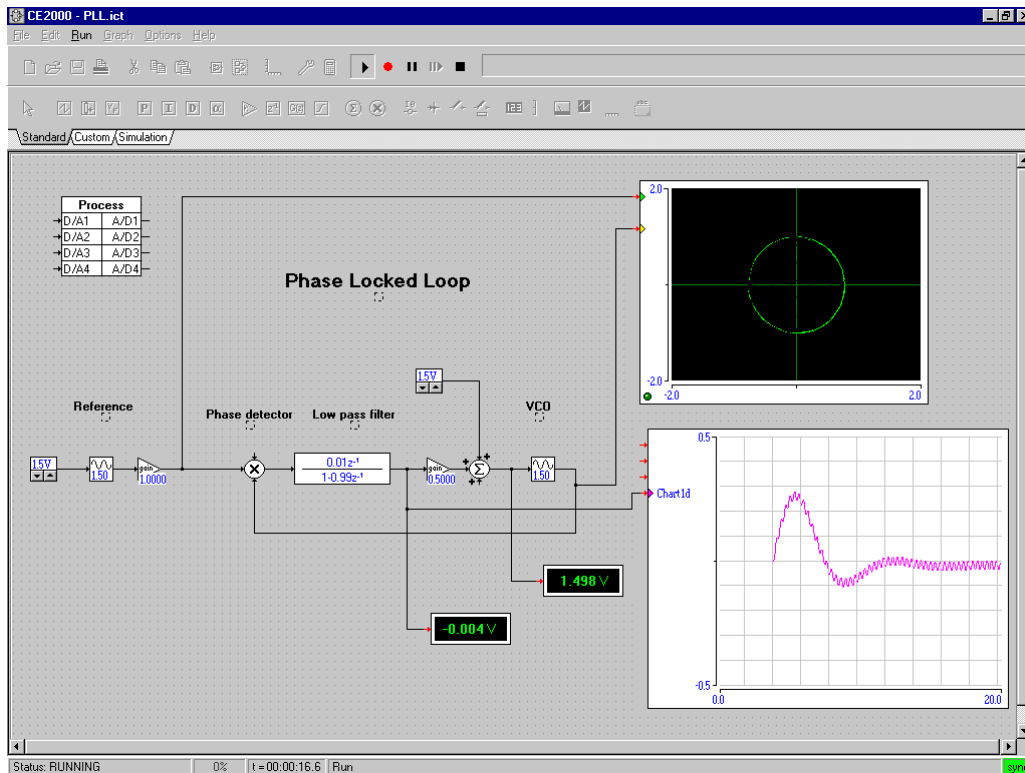


Figure 4. CE2000 Implementation of a PLL

4. Practical Performance of a Phase Locked Loop

To make the experiment more realistic the above PLL CE2000 implementation is driven by an external reference signal. When the simulation is started the PLL locks to the incoming reference signal. When steady state is reached the frequency of the reference oscillator is increased and the PLL locks to the new reference frequency. In this CE2000 program the AD/DA block is selected to have only one input and one output. This allows the sampling time to be set to 15 ms. The experimental set up and the CE2000 implementation are shown in figure 5, on the next page.

5. A Final Word

It is not possible to answer questions about our white papers, unless we have a contract with your organisation. For more information about the CE2000 Control and Simulation Software go to the TQ Education and Training web site using the links on our web site www.control-systems-principles.co.uk or use the email info@tq.com. There are many books on phase locked loops and tutorial papers. We are particularly indebted to the references listed below.

6. References

1. Daniel Abramovitch, Phase-locked loops: a control tutorial, Proc ACC, Anchorage, May 2002.
2. Dorf, R C and Bishop, R H, Modern Control Systems, (9th Ed) Prentice Hall 2000.
3. WWW. There are lots of resources on PLL design and applications on the www. Many of deal with radio frequency (RF) design and applications.

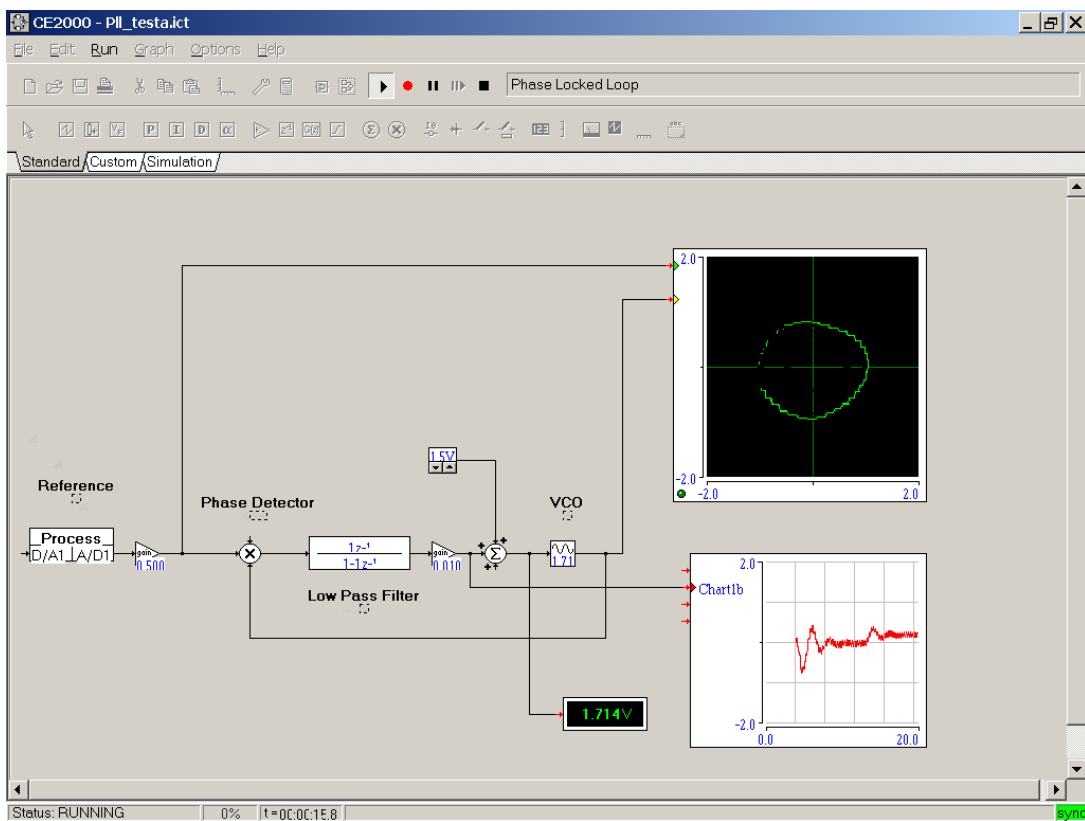
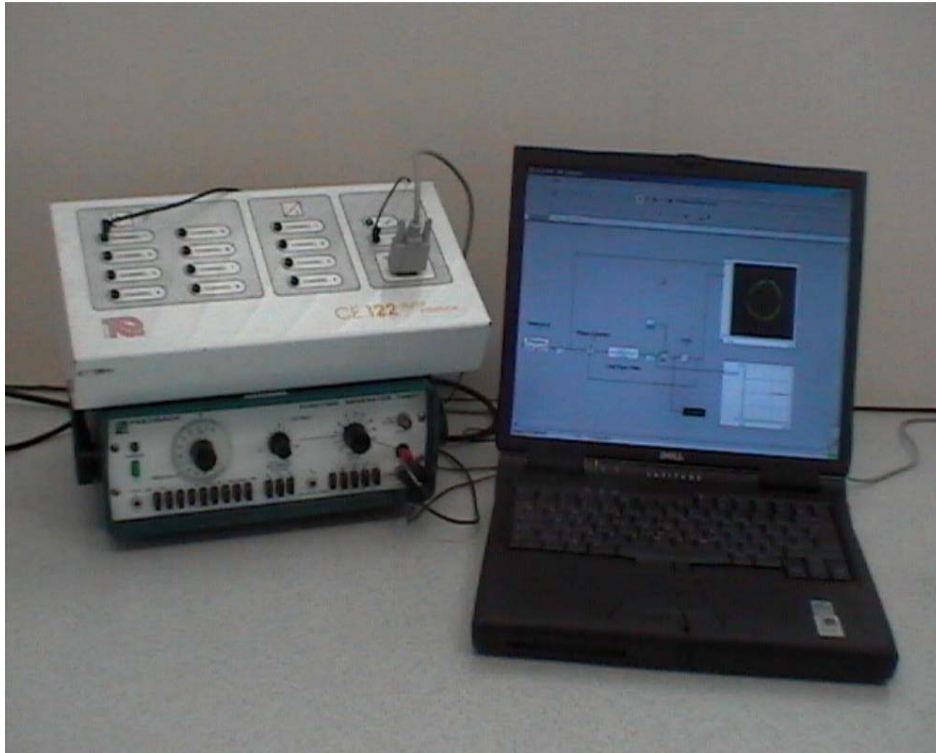


Figure 5. (Top) Experimental arrangement, (Bottom) CE2000 implementation of a PLL